REMARKS/ARGUMENTS

Claims 9-12 are pending, with all claims being amended. No new subject matter is added in the amended claims.

The Examiner finally rejects claims 9-12 under 35 U.S.C. 103(a) as being unpatentable over Yukio (JP 2-294061). The Examiner admits that although the Yukio reference does not classify the two chips as either master or slave as in the claimed invention, it is clear that the overall structure is generic to all types of chips. From this, the Examiner states that it would have been obvious to one having skill in the art to use the frame in the prior art for master/slave or any other circuits associated with testing, since semi-conductor chips function differently and that lead frames serve as the base carrier element for different types of chips because of the art recognized reliability in stabilizing semiconductor chips.

Applicant has carefully reviewed the Yukio reference, and respectfully traverses this ground of rejection. Applicant respectfully believes that the Examiner, in reaching the above conclusions, reads into this reference that a user will, by selectively providing a wire lead 15 between a chip 11 or 12 and leads 13, provide a chip package such that two chips function in a drive/master or receiver/slave chip relationship. However, Applicant fails to find any teaching or suggestion in Yukio for this. Indeed, Figures 1 and 2 show the chips as having the same size, shape and bonding pads connected to the same number of external leads 13 and internal leads 16. It is thus pure conjecture on the part of the Examiner that one of the chips 11 or 12 would be a slave chip and one would be a master chip. Indeed,

the arrangement of the two IC chips in Yukio has the appearance of memory IC's which are joined together in banks.

The Examiner further states that the Taniguchi et al. reference discloses an IC with an embedded test circuit as taught in the abstract. The abstract further states, however, that "a logic IC including an embedded memory is provided with a test circuit therein which allows the embedded memory to be tested by using only 3 additional external pins of the logic IC for test purposes without regard to the bit count of the unit in which data is written into and read out from the embedded memory." Individual IC chip can have different sections which can be considered separate "circuits" with different functions. This is not, however, equivalent to the claimed invention, where a separate master IC chip tests a separate slave IC chip with both IC chips residing in the same semiconductor chip package.

Independent claim 9 recites a semi-conductor chip package "wherein said master integrated circuit chip includes an embedded testing circuit to permit testing of said slave integrated circuit chip that is connected thereto during a testing process of said semiconductor chip package." As discussed above, this feature is neither taught nor suggested by Yukio or Taniguchi et al. Accordingly, Applicant believes that claim 9 is unobvious.

Turning next to the rejection of dependent claim 11, claim 11 is amended to recite that "there are no external connection leads electrically connected to any bonding pads on said slave integrated circuit chip, said external connection leads serving as terminal pins such that external electrical connection with said slave integrated circuit chip is established only via said master integrated circuit chip." Referring back to the Yukio reference,

its FIGS. 1 and 2 clearly show two chips 11 and 12, with the same size, shape and bonding pads connected to the same number of external leads 13 and internal leads 16. It is thus clear the Yukio reference does not teach or suggest the claimed limitation. The limitations of claim 12 that "said master integrated circuit chip is configured to receive stimulating signals via said external connection leads to stimulate said at least one slave integrated circuit chip via said internal connection leads in response to the stimulating signals, to receive stimulation response of said at least one slave integrated circuit chip via said internal connection leads, and to output information corresponding to the stimulation response via said external connection leads" is likewise not taught or suggested by the Yukio or Taniguchi et al. references. The Examiner's statement that Taniguchi et al. teaches an IC with an embedded test circuit (that tests itself) does nothing to advance the argument that this teaches the claimed invention since Taniguchi et al. neither teaches nor suggests that a separate master integrated circuit chip that is connected to external leads is used to test a slave integrated circuit chip, where both chips are in the same chip package.

For the above reasons, Applicant respectfully submits that each of claims 9-12 recites patentable subject matter, and requests allowance of same. Particularly since this paper is in response to a final office action, if the Examiner has any questions or

alternate suggestions, a telephone call to the undersigned would be appreciated.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

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